WHAT IS CLAIMED IS:

1. A ferroelectric memory device comprising:

memory cells each having a cell transistor having a source terminal and a drain terminal and a ferroelectric capacitor in between said two terminals;

a memory cell block including the memory cells that are series connected between a first terminal and a second terminal, the first terminal being connected to a bit line via a block select transistor, the second terminal being connected to a plate line, and the cell transistor having a gate connected to a word line;

a sense amplifier which amplifies data read out from the memory cell to the bit line, and generates one of a first potential and a second potential higher than the first potential in accordance with the read-out data;

a precharge circuit which precharges the bit line at a third potential that is higher than the first potential and lower than the second potential;

a bit line drive circuit which sets the bit line precharged by the precharge circuit at a fourth potential; and

a plate line drive circuit which supplies a potential to the plate line.

2. The ferroelectric memory device according to claim 1, wherein the plate line drive circuit precharges the plate line at a fifth potential that is

higher than the first potential and lower than the second potential.

3. The ferroelectric memory device according to claim 2, wherein the fifth potential is equal to the third potential.

4. The ferroelectric memory device according to claim 1, wherein a potential difference between the first potential and the third potential is substantially equal to 1/2 of a potential difference between the first potential and the second potential.

5. The ferroelectric memory device according to claim 1, wherein the bit line drive circuit includes:

a transistor with a current path having one end connected to the bit line; and

a capacitor element having one electrode connected to the other end of the current path of the transistor and having the other electrode connected to the first potential.

6. The ferroelectric memory device according to claim 1, wherein the bit line drive circuit includes:

a capacitor element having one electrode connected to a drive potential; and

a switching element which connects the other electrode of the capacitor element to one of the first potential and the bit line, the bit line being set at a predetermined potential by control of the drive potential.

7. The ferroelectric memory device according to claim 1, wherein the bit line drive circuit includes a transistor with a current path having one end connected to the bit line and having the other end connected to the first potential.

8. The ferroelectric memory device according to claim 1, wherein the bit line drive circuit sets a potential of the bit line at the fourth potential, immediately before data is read out of the memory cell, and

a potential difference between the third potential and the fourth potential is greater than a potential variation amount of the bit line when "0" data has been read out of the memory cell and is less than a potential variation amount of the bit line when "1" data has been read out of the memory cell.

9. A data read-out method for a ferroelectric memory device which consists of series connected memory cells each having a transistor having a source terminal and a drain terminal and a ferroelectric capacitor in between said two terminals, the method comprising:

precharging at a first potential a first bit line connected via a block select transistor to one end of a memory cell block including the series connected memory cells, and precharging at a second potential a plate line connected to the other end of the memory cell block;

reading out data from the memory cell to the first bit line; and

amplifying a potential of the first bit line to one of a third potential that is lower than the first potential and a fourth potential that is higher than the first potential, in accordance with the data read out of the memory cell.

10. The data read-out method according to claim 9, further comprising:

precharging a second bit line at the first potential before the reading-out of data to the first bit line; and

setting the first bit line at a fifth potential,

wherein the amplifying of the potential of the first bit line to one of the third potential and the fourth potential includes amplifying the potential of the first bit line to the third potential when the potential of the first bit line is lower than the potential of the second bit line when data has been read out of the memory cell, and amplifying the potential of the first bit line to the fourth potential when the potential of the first bit line is higher than the potential of the second bit line when data has been read out of the memory cell.

11. The data read-out method according to claim 10, wherein the setting of the first bit line at the fifth potential includes applying a control signal

to one electrode of a capacitor element, the other electrode of which is electrically connected to the first bit line, and controlling the potential of the first bit line by coupling of the capacitor element.

12. The data read-out method according to claim 9, wherein the first potential is equal to the second potential.

13. The data read-out method according to claim 9, wherein a potential difference between the third potential and the first potential is substantially equal to 1/2 of a potential difference between the third potential and the fourth potential.